Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) An application specific integrated circuit (ASIC) comprising:

a standard cell~~, the standard cell~~ including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) ~~function~~ coupled to the at least one bus and the plurality of internal signals, the field programmable gate array (FPGA) ~~function~~ including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals, the debug client function being in communication with a server and including,

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the field programmable gate array (FPGA) with a trigger pattern downloaded from the server; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

2. (Currently Amended) The ASIC of claim 1, wherein the at least one bus comprises an internal bus, the internal bus being internal to the ASIC and not being exposed via an I/O pin.

3. (Currently Amended) The ASIC of claim 2, wherein the ~~debug client function observes and manipulates at least one of the plurality of logic functions on the standard cell~~ server comprises a debugger server running a debugger application.

4. (Currently Amended) The ASIC of claim ~~1~~ 3, wherein the debug client function is programmed by a the debugger server.

5. (Currently Amended) The ASIC of claim 1, wherein the debug client function further includes:

~~an~~ external communicator logic ~~function~~ for receiving and transmitting information to a the server;

selector logic coupled to the at least one bus and the plurality of internal signals, the selector logic to provide each one of the plurality of internal signals coupled to the field programmable gate array (FPGA) at a particular input point within the debug client function; and

~~an~~ interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween.

6. (Currently Amended) The ASIC of claim 5, wherein the interface logic comprises:

a the storage logic ~~function for storing a state of at least one signal from the selector logic and providing the state to a server~~;

a the comparator logic, wherein the comparator logic ~~function~~ is coupled to the storage logic ~~function for comparing the at least one signal from the selector block function~~; and

~~an~~ output logic ~~function~~ coupled to the comparator logic ~~function~~ for controlling the plurality of internal signals on the ASIC.

7. (Currently Amended) The ASIC of claim 4, wherein the server utilizes the debug client function to debug hardware within at least one of the plurality of logic functions.

8. (Currently Amended) The ASIC of claim 4, wherein the server utilizes the debug client function to debug software within at least one of the plurality of logic functions.

9. (Currently Amended) A debug client function within an application specific integrated circuit (ASIC), the debug client function being within a field programmable gate array (FPGA) ~~function~~, the client debug function comprising:

~~an~~ external communicator logic ~~function for receiving and transmitting information concerning a plurality of internal signals of the ASIC to~~ in communication with a server;

selector logic coupled to ~~at least one bus of the ASIC and the~~ a plurality of internal signals that are internal to the application specific integrated circuit (ASIC) and not being exposed via an I/O pin, the selector logic to provide each one of the plurality of internal signals coupled to the field programmable gate array (FPGA) at a particular input point within the debug client function;

comparator logic operable to compare selected ones of the plurality of internal signals at the particular input point with a trigger pattern downloaded from the server through the external communicator logic; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server through the external communicator logic.

~~an interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween,~~

~~wherein the at least one bus comprises an internal bus, and the debug client function observes and manipulates at least one of the plurality of internal signals of the ASIC.~~

10-11. (Cancelled)

12. (Currently Amended) The ~~ASIC~~ debug client function of claim 9, wherein the debug client function is programmed by a the server.

13. (Cancelled)

14. (Currently Amended) The ~~ASIC~~ debug client function of claim 12, wherein the server utilizes the debug client function to debug hardware within at least one of the plurality of logic functions.

15. (Currently Amended) The ~~ASIC~~ debug client function of claim 12, wherein the server utilizes the debug client function to debug software within at least one of the plurality of logic functions.

16-19. (Cancelled)

20. (New) An application specific integrated circuit (ASIC) comprising:

a standard cell including a plurality of logic functions and a plurality of software interfaces; and

a field programmable gate array (FPGA) internally connected to one or more internal signals associated with the plurality of logic functions and connected to one or more of the plurality of software interfaces, each internal signal not being exposed via an I/O pin, the field programmable gate array (FPGA) including,

a debug client function operable to observe and manipulate each internal signal and manage instruction pointer logic associated with the one or more software interfaces connected to the field programmable gate array (FPGA).

21. (New) The ASIC of claim 20, wherein the debug client function manages instruction pointer logic including manipulating one or more registers and memories associated with the one or more software interfaces connected to the field programmable gate array (FPGA).

22. (New) The ASIC of claim 21, wherein the debug client function is triggered based on software values.